We claim:

1. A process for producing a doped semiconductor substrate, which comprises the following steps:

providing a semiconductor substrate;

producing a doping at a surface of the semiconductor substrate;

applying a layer selected from the group consisting of a polycrystalline layer and an amorphous layer to the surface; and

carrying out a heat treatment step for producing an epitaxial layer and a buried doping.

2. The process according to claim 1, which comprises during the applying step, forming the amorphous layer to extend a predetermined depth into the semiconductor substrate, and is produced by ion bombardment.

3. The process according to claim 2, which comprises carrying out the ion bombardment with at least one ion type selected from the group consisting of germanium ions, silicon ions and noble gas ions.

4. The process according to claim 2, which comprises forming the amorphous layer to have a thickness of between 500 - 1000 nm.

5. The process according to claim 1, which comprises performing a rapid thermal annealing process before carrying out the heat treatment step.

6. The process according to claim 5, which comprises carrying out the rapid thermal annealing process out at a temperature of between 1000° and 1100° C.

7. The process according to claim 5, which comprises carrying out the rapid thermal annealing process for a time period of between 10 and 60 seconds.

8. The process according to claim 1, which comprises forming the semiconductor substrate from silicon.

9. The process according to claim 1, which comprises forming the polycrystalline layer and the amorphous layer from silicon.

10. The process according to claim 1, which comprises producing the doping by an ion implantation process.

11. The process according to claim 9, which comprises carrying out the ion implantation process using ions selected from the group consisting of B, P, As, In and Sb ions.

12. The process according to claim 1, which comprises depositing a poly/α layer using a low-pressure chemical vapor deposition process to the surface of the semiconductor substrate.

13. The process according to claim 12, which comprises depositing the poly/α layer at a low temperature.

14. The process according to claim 12, which comprising forming the poly/α layer to have a thickness between 20 nm to 40 nm.

15. The process according to claim 12, which comprises carrying out a crystallization of at least one of the amorphous layer and the poly/α layer by performing a low-temperature step.

16. The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of between 600° C to 700° C.

17. The process according to claim 15, which comprises carrying out a wet etching operation out after performing the low-temperature step.

18. The process according to claim 15, which comprises performing the crystallization at a same time as a formation of a gate oxide.

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~~19~~. The process according to claim 12, which comprises depositing the poly/α layer at a temperature of between 500° C and 600° C.

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~~20~~. The process according to claim 15, which comprises carrying out the low-temperature step at a temperature of 650° C.